

Laboratory Experiments for Introductory and Advanced VLSI Courses

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Abstract

This paper focuses on the experimental design of large scale integrated circuits (LSICs) by senior and graduate level students at Missouri University of Science and Technology. We have designed a series of experiments to teach fundamentals of full-custom IC design, which include front-end to back-end flow. These labs help IC beginners understand the entire full-custom design process. Labs are executed in both an undergraduate and advanced graduate course. The lab experience includes projects. An example project – a 100 MHz output clock phase-lock loop (PLL) with 10 MHz input – will be discussed. In this lab, students use Virtuoso schematic editor to develop each portion of the PLL: the phase detector, charge pump, filter, voltage controlled oscillator, and a divider. The sizes of FETs are determined based on simulation results. Three kinds of divider structures are tested to find the one which provides the best performance. After the design passes front-end simulation, the students implement the layout of these modules in the layout editor, and DRC and LVS are executed to verify their design. Finally, post-simulation is used to prove the PLL works well in a long time simulation in the presence of layout parasitics and noise. Completion of these labs significantly improves the students' understanding of the basic full-custom design flow.

Introduction to PLL Design

The Phase Locked Loop (PLL) generates a high-frequency internal clock signal with fixed phase with respect to a lower-frequency reference clock. A typical PLL is shown in Figure. 1, which is composed of several components: phase detector, charge pump followed by a filter, and then a VCO unit, which is the core of PLL.

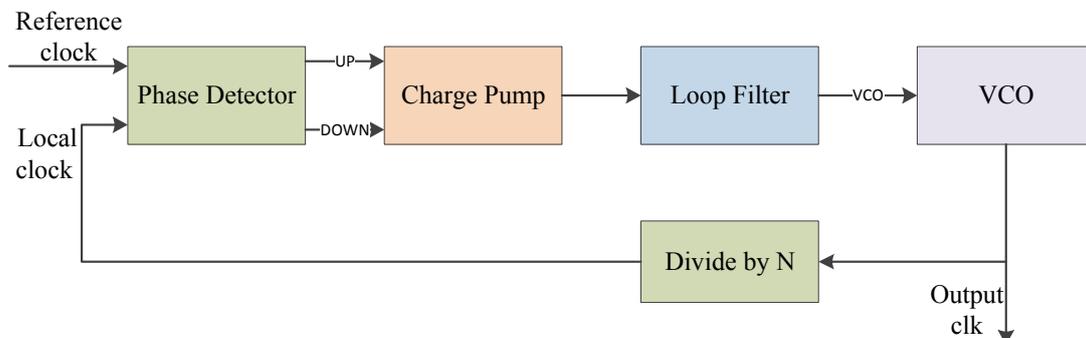


Figure 1 Structure of PLL

The proposed circuit structure for each component is as follows:

- A register phase detector which samples the clock at the rising edge of the clock is recommended. This detector has no requirement for the duty cycle of the clock, which will make the design of the divider easier.
- For the charge pump, a differential structure will have better performance, and significantly reduce the influence of power-supply noise.
- A very simple loop RC filter can fulfill the loop-filter requirement.
- A current starved inverter structure is recommended for the voltage controlled oscillator. Seven inverters could be used to generate a 100MHz clock.
- The divider is used to generate a feedback clock to the phase detector. The divider is composed of four D flip-flops. The input is a ~100MHz clock, and the output is a ~10 MHz clock. The 10 MHz clock is compared with the reference clock input.

Technical Accomplishments

Through this experimental design of very large scale integrated (VLSI) circuits, the students master the fundamentals of industrial-strength full-custom IC design tools, and develop a solid understanding of the digital and analog design issues in a basic PLL circuit. They learn how to do front-end design, simulation, back-end layout, design-rule check (DRC), layout-versus-schematic (LVS), post-layout simulation, and more. This practical design experience also helps improve their understanding of basic design principles and theory taught in the class. For example, how the difference between NMOS carrier mobility and PMOS will cause asymmetries in transmission time and how to design a faster circuit considering logic effort, and more.

Design Lessons Learned

In this experiment, the students are allowed to choose their own circuit structure and are not required to follow proposed structure above. Some students, however, do not consider the layout complexity at the schematic design phase, and then they encounter significant difficulties at the back end post layout design. It is important to give them more overall guidance at the schematic design phase to prevent these problems. Highlighting key design rules in advance, such as logic effort and symmetry design, will also help students get their design to work.

References

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2. Virtuoso Analog Design Environment XL User Guide Product Version 6.1.5 July 2012, www.cadence.com
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Bibliographical Information

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Design of an Antipodal Vivaldi Antenna for use in a Bi-Static Linear Array



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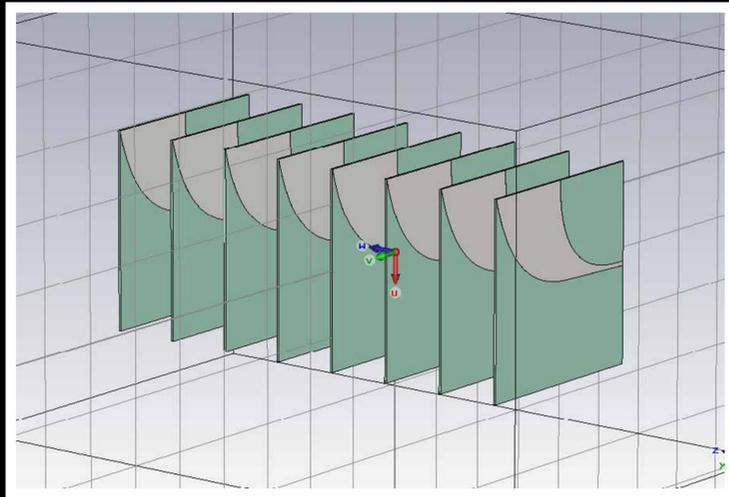
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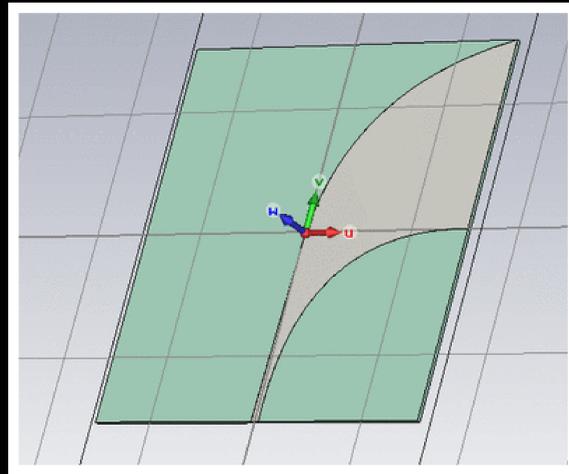


Ultra Wide Band Imaging

UWB microwave imaging techniques (0.3-300GHz) provide a method to locate objects, flaws, and other discontinuities behind or within a dielectric medium. With multiple antennas in a bi-static linear phased array, the data can be efficiently collected and processed to construct through-wall (concrete structures) and sub-surface (soil) images.



Concept Design of Antenna Array



Design of Antenna using CST

Simulation of Antenna

CST-MWS [1] design software was used to simulate the antenna, fabricated as a copper clad PCB with FR-4 substrate construction. The PCB design optimizes performance within the stated constraints, offering wide bandwidth and narrow profile. Software simulation allowed for exploration of such performance-optimizing parameters such as exponential taper, variation of line feed, and antenna dimensions [2],[3].

Prototype Antenna Construction

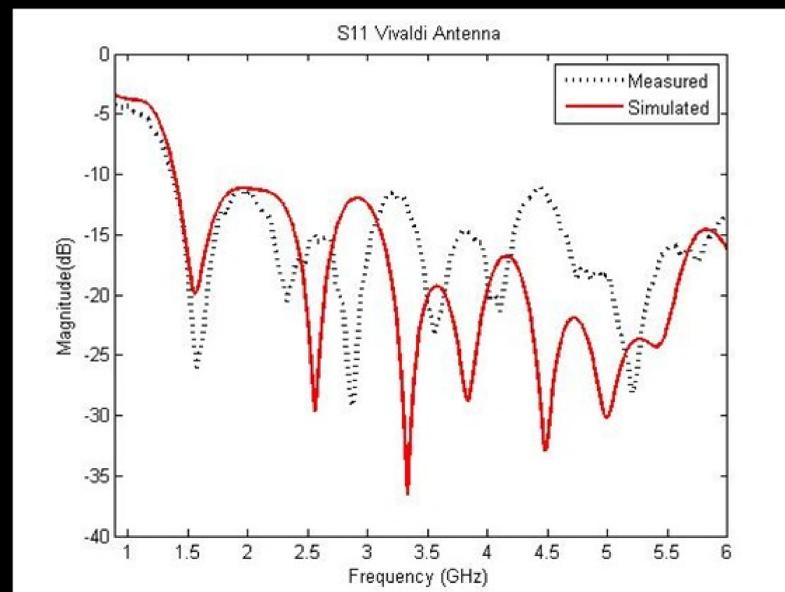
The taper design was printed from the successful simulation, and masked onto a copper clad FR-4 PCB. Ferric acid was used to etch the cladding. An SMA edge-launch connector was soldered to the end of the line feed strip.



Completed Vivaldi prototype antenna

Antenna Design Constraints

An antenna for use in this array design must have a narrow profile while being able to achieve high directivity across a large bandwidth. In order to construct the desired images, the antennas must also optimize low frequency performance without general forfeit of resolution. This trade off was considered optimal at a 150 mm width, which should ideally reach across a frequency bandwidth of 1-6 GHz. The upper bound is limited by the Vector Network Analyzer (VNA) used to provide the excitation signal. The lower bound will be determined by the antenna width, 150 mm, which provides a theoretical floor of 1GHz.



Reflection coefficient characteristics by frequency, comparing simulation vs. prototype

Conclusion

The completed prototype performed consistently with the simulation across the desired range of frequencies. The S_{11} characteristics for both the simulation and prototype indicate a functional low frequency range down to 1.4 GHz.

References

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- [2] Giuseppe Ruvio, Domenico Gaetano, Max J. Ammann, and Patrick McEvoy, "Antipodal Vivaldi Antenna for Water Pipe Sensor and Telemetry," *International Journal of Geophysics*, Volume 2012 (2012), Article ID 916176, 8 pages
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